IN THE SPECIFICATION

Please replace the title appearing on the first page of the present specification with the following title as rewritten:

SEMICONDUCTOR PACKAGE WITH HEAT SINK~~FAN-OUT SEMICONDUCTOR CHIP ASSEMBLY~~

Please replace paragraph [0038] of the present specification with the following rewritten paragraph:

[0038] Each first lead 62 has a terminal end 68 (Fig. 3) permanently attached to the bottom of sheet 52 and a tip end 70 remote from such terminal end releasably attached to the bottom surface of the sheet. The permanent attachment may be constituted by a metallurgical bond between the terminal ends 68 and the vias 60a, 60b and 60c extending through the sheet or into the sheet from the bottom surface 56. The structure of these leads may be the same as described in the aforementioned '964 Patent. Merely by way of example, leads 62 may have curved sections extending between the tip ends and the terminal ends. The second leads 64, in peripheral region 59, have a generally similar configuration. Thus, each such second lead has a terminal end 72 permanently attached to the sheet and a tip end 74 releasably attached to the sheet bottom surface 56. Each of the tip ends 70 and 74 may have bonding material thereon. The bonding materials may be eutectic bonding alloys or other materials which can be captivated upon exposure to elevated temperature and which form a solid bond with the leads and contacts. For example, where the lead tip ends and the chip contacts include gold, the bonding material may include tin silicon or alloys thereof with gold. Many other bonding materials are described in the '964 Patent, and can be used in the present invention.

Please replace paragraph [0053] of the present specification with the following rewritten paragraph:

[0053] In a further embodiment of the invention, the dielectric element 352 (Fig. 15) is a substantially rigid, substantially imperforate dielectric plate formed from a ceramic material. As used in this disclosure with reference to a dielectric element, the term "substantially imperforate" means that at least the central region of the dielectric element overlying the chip 320 is devoid of holes extending between the top surface 354 and the bottom surface 356, or that any holes extending between the top and bottom surfaces are filled by via liners or other conductive elements. Because plate 352 is substantially imperforate, it shields the chip and the associated flexible leads 362 extending between the chip and the dielectric element. As in the embodiments discussed above, the dielectric element has terminals 358 disposed on the top surface 354 (the surface facing away from chip 320). These terminals are arranged in a "fan-out" pattern, so that the terminals are disposed in the peripheral region of the dielectric element, outside of the central region aligned with the chip. The terminals are connected to the chip contacts through flexible leads 362 and horizontal conductors 366 extending within plate 352, on the surfaces of the plate, or both. The package element includes a metallic plate heat spreader 350 secured to the rear surface of the chip by a thermally conductive adhesive 351. Plate 350 extends parallel to plate 352, with the chip disposed therebetween, and with a compliant dielectric layer 390 filling the remaining space between the plates and intimately surrounding flexible leads 362. The plates and the dielectric layer cooperatively protect the chip. The assembly can be handled and mounted readily using conventional surface mounting techniques. Thus, terminals 358 may be provided with bonding materials such as solder balls. As depicted in Fig. 15, the assembly is mounted to a substrate 370, with terminals 358 bonded to contact pads 359 on the substrate by conventional

bonds such as solder masses. Substrate 370 desirably has a coefficient of thermal expansion closely matched to the coefficient of thermal expansion of plate 352, so as to minimize differential thermal expansion of these elements. The flexible leads 362 compensate for differential thermal expansion or movement between chip 320 and plate 352.